



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,731	12/16/2003	Ho Uk Song	29936/39880	3574
4743	7590	12/14/2004	EXAMINER	
MARSHALL, GERSTEIN & BORUN LLP 6300 SEARS TOWER 233 S. WACKER DRIVE CHICAGO, IL 60606			NGUYEN, HIEP	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/736,731

Applicant(s)

SONG, HO UK

Examiner

Hiep Nguyen

Art Unit

2816



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 6-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12-16-03 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the “delay circuit is added to an output terminal of the off-chip driver” in claim 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not). Claim 5 is missing.

Claim 3 is objected to because of the following informalities: it is not clear if the delay circuit is added to the input terminal or to the output terminal of the off-chip driver. Figure 2 of the present application shows that the delay circuit is added to the input terminal of the off-chip driver.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4, 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation “ a signal” on line 6 is indefinite because it is not clear as to this “a signal” is the same or different than the “a data signal” on line 2. It is not clear what the “other signals” is meant by.

Regarding claims 4 and 8, the recitation “ wherein each of the off-chip drivers performs an NAND operation for a corresponding control signal and the data signal when a logical status of the inputted data signal is High and an NOR operation for an inverse signal of a corresponding control signal and the data signal when a logical status of the inputted data signal is Low” is indefinite because it is misdescriptive. Figure 3 and 4 of the present application shows the off-chip drivers comprising NAND gate and NOR gate. Thus, the off-chip driver always perform an NAND operation or an NOR operation independent from the levels of the input signals.

Regarding claim 9, the recitation “wherein the output driver circuit comprises each of the output drivers and off-chip drivers corresponding to the pre-driver circuit, wherein, if a control signal.” is indefinite because it is not clear what the “each of the output driver” is meant by. Figure 2 of the present application shows that the off-chip driver and the pre-driver circuit are **separate** circuits thus, the recitation “each of the output drivers and off-chip drivers corresponding to the pre-driver circuit” is confusing. The recitation “if” is not a positive recitation. It should be changed to “when”.

Claims 2 and 3 are indefinite because of the technical deficiencies of claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Watkins et al. (US Pat. 6,359,483).

Regarding claims 1, 2 and 3, figure 2 of Watkins shows an off-chip driver circuit having first to Nth off-chip drivers for using a data signal and first to Nth control signals respectively to determine whether to produce output signals according to corresponding control signals, being characterized in that:

at least one of the first to Nth off-chip drivers comprises a delay circuit (128) for outputting a signal having a given delay time compared with other signals of the remaining off-chip drivers. The delay circuit (128) is added to the input terminal of the off-chip driver.

Regarding claims 6, figure 2 of Watkins shows a data output circuit comprising:

first to Nth off-chip drivers (144-156) for outputting a data signal, respectively, in response to first to first to first to Nth control signals;

a pre-driver circuit (142) for using the data signal to drive an output driver circuit (multiple input NAND gate); and

the output driver circuit connected to the outputs of the off-chip driver circuit (144-156) and the pre-driver circuit (142),

wherein, at least one of the first to first to Nth off-chip drivers comprises a delay circuit (128) for delaying the data signal.

Regarding claim 7, the pre-driver circuit (142) is a NAND gate. The built in pull-up/down circuit pulls the data up/down.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2816

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins et al. (US Pat. 6,359,483).

Regarding claim 4 and 8, figure 4 of Watkins shows the off-chip drivers (142...156) are NAND gates thus, they perform the NAND function independent of the levels of the input signals. The control signals are the outputs of the flip-flops. Figure 4 of Watkins does not show that the off-chip drivers are NOR gates. However, the NAND gate and NOR gate are interchangeable according to the Boolean algebra, it is well know that the NAND gate can be replaced with an NOR gate for layout convenience. Therefore, it would have been obvious to those skilled in the art to use a circuit comprising all NAND gates of all NOR gates for easy layout and for reducing cost.

Regarding claim 9, the output driver circuit (the multiple input NAND gate) internally comprises a plurality of "output drivers" that receive the outputs from the off-chip drivers as control signals as enable signals.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2816

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

12-08-04



TUAN T. LAM
PRIMARY EXAMINER